

External Memory Address Map

2764(64kbit PROM) or 6264(64kbit SRAM)  
 ROM / Read / Write (6264 only)  
 IC11[0000-1FFF] / LT[0000-1FFF] / W[0000-1FFF]  
 IC12[0000-1FFF] / LT[2000-3FFF] / W[2000-3FFF]  
 IC18[0000-1FFF] / RT[0000-1FFF] / W[4000-5FFF]  
 IC19[0000-1FFF] / RT[2000-3FFF] / W[6000-7FFF]

27128(128kbit PROM)  
 ROM / Read  
 IC11[0000-1FFF] / LT[0000-1FFF]  
 IC12[0000-1FFF] / LT[2000-3FFF]  
 IC11[2000-3FFF] / LT[4000-5FFF]  
 IC12[2000-3FFF] / LT[6000-7FFF]  
 IC18[2000-3FFF] / RT[0000-1FFF]  
 IC19[2000-3FFF] / RT[2000-3FFF]  
 IC18[0000-0FFF] / RT[4000-5FFF]  
 IC19[0000-0FFF] / RT[6000-7FFF]

Left Read / Write

EN245	19	OE	VCC	20
RD0	1	DIR	VCC	20
DB8	2	A1	B1	18
DB7	3	A2	B2	17
DB0	4	A3	B3	16
DB5	5	A4	B4	15
DB1	6	A5	B5	14
DB4	7	A6	B6	13
DB2	8	A7	B7	12
DB3	9	A8	B8	11
DL6	18			
DL7	17			
DL0	16			
DL1	15			
DL2	14			
DL3	13			
DL4	12			
DL5	11			

Left Mirror Read

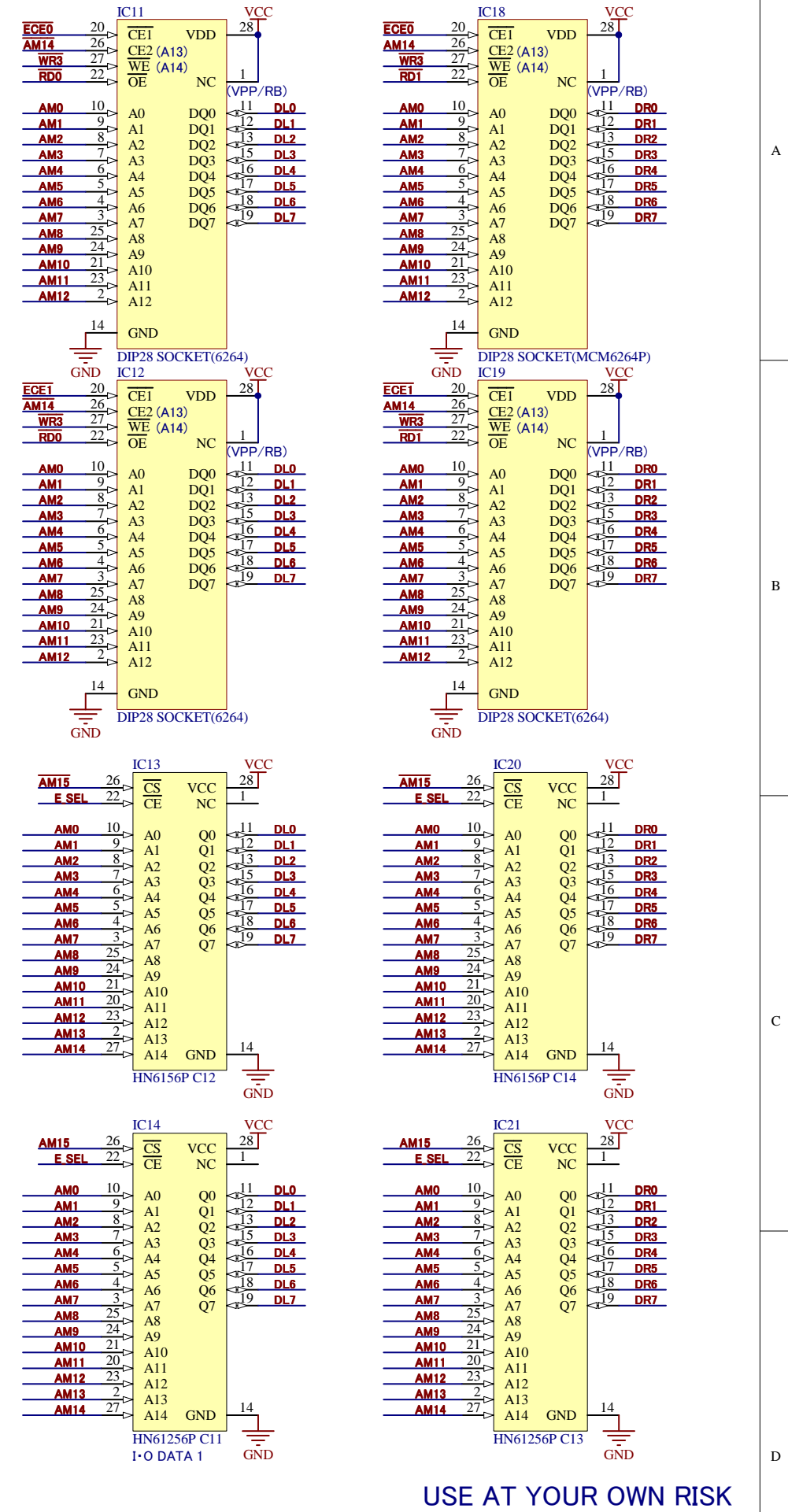
RD2	1	1OE	VCC	19
RD2	1	2OE	VCC	19
DB1	18	1Y1	1A1	2
DB0	16	1Y2	1A2	4
DB2	14	1Y3	1A3	6
DB3	12	1Y4	1A4	8
DB4	9	2Y1	2A1	11
DB5	7	2Y2	2A2	13
DB6	5	2Y3	2A3	15
DB7	3	2Y4	2A4	17
DL6	2			
DL7	4			
DL0	6			
DL1	8			
DL2	11			
DL3	13			
DL4	15			
DL5	17			
DLO	19			

Right Read/Write

EN245	19	OE	VCC	20
RD1	1	DIR	VCC	20
DB7	2	A1	B1	18
DB6	3	A2	B2	17
DB0	4	A3	B3	16
DB5	5	A4	B4	15
DB1	6	A5	B5	14
DB4	7	A6	B6	13
DB2	8	A7	B7	12
DB3	9	A8	B8	11
DR7	18			
DR6	17			
DR0	16			
DR1	15			
DR2	14			
DR3	13			
DR4	12			
DR5	11			

Right Mirror Read

RD3	1	1OE	VCC	19
RD3	1	2OE	VCC	19
DB0	18	1Y1	1A1	2
DB1	16	1Y2	1A2	4
DB2	14	1Y3	1A3	6
DB3	12	1Y4	1A4	8
DB4	9	2Y1	2A1	11
DB5	7	2Y2	2A2	13
DB6	5	2Y3	2A3	15
DB7	3	2Y4	2A4	17
DR0	2			
DR1	4			
DR2	6			
DR3	8			
DR4	11			
DR5	13			
DR6	15			
DR7	17			



USE AT YOUR OWN RISK  
 This schematic was written by the trace of the real PCB.  
 There is no warranty of any kind.